International Journal of Electronics Communication and Computer Engineering
Volume 4, Issue 2, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

Survey and Evaluation of D Flipflop for Low Power Counter Design Using Sub-Micron Technology

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***Abstract* — As chip manufacturing technology is on the threshold of major evaluation, which shrinks chip size and performance, LFSR is implemented in layout level which develops low power consumption chip, using recent CMOS, sub-micrometer layout tool. This paper compares various architectures in terms of hardware implementation, power consumption, and CMOS layout using Microwind tool. Thus it provides a low power architecture implementation of LFSR counter using Microwind. The Microwind tool allows the designer to design and simulate an integrated circuit at physical description level.**

***Keywords* — LFSR Counter, Layout Generation, Physical Description, Pass Transistors, CMOS Topologies.**

I. INTRODUCTION

Due to advancements in large scale integration, millions of transistors can be placed on a single chip for implementation of complex circuitry. As a result of placing so many transistors in such a small space, major problems of heat dissipation and power consumption have come into the picture. Research has been conducted to decrease the power supply voltage, switching frequency and capacitance of transistor [1]. LFSR is used in a variety of applications such as Built-in-self test (BIST) [7].

Today LFSR’s are present in nearly every coding scheme as they produce sequences with good statistical properties, and they can be easily analysed. Moreover they have a low-cost realization in hardware. Counters such as Binary, Gray suffer problem of power consumption, glitches, speed, and delay because they are implemented with techniques which have above drawbacks. They produce not only glitches, which increase power consumption but also complexity of design. The propagation delay of results of existing techniques is more which reduces speed & performance of system. For layout and simulation at deep submicron CMOS design tool Micro wind is used.

LFSR can be used as a fast counter, if the particular sequence of count values is not important. It can be used as a random number generator and also to generate pseudorandom sequence. The sequence gets repeated for every 2^n-1 patterns. LFSR finds variety of application in computer graphics, cryptography, automatic testing for error detection and correction, and in CRC (cyclic redundancy codes).

II. LINEAR FEEDBACK SHIFT REGISTER

An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit. LFSRs are frequently used as pseudorandom pattern generators to generate a random number of 1s and 0s.

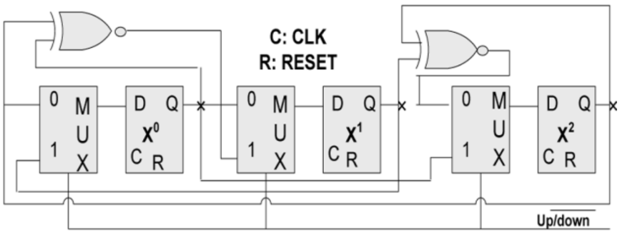

Fig.1. Three bit maximum length up/down counter

Each output of the LFSR [9] is multiplexed with an ASIC input and, when the device is placed in the LFSR (test) mode, the random, high-toggle-rate patterns produced are extremely good for generating high-fault coverage. A LFSR can be formed by performing exclusive-NOR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip flops as shown in Fig.1. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the sequence of values produced by the register is completely determined by its current (or previous) state.

A. Working of LFSR:

A maximum length n-bit LFSR sequences through 2^n-1 states. It goes through all possible code permutations except one. The LFSR consists of a shift register and a few embedded XNOR gates fed by a feedback loop [4]. Each LFSR has the following defining parameters:

- Width, or size, of the LFSR (it is equal to the number of bits in the shift register);
- Number and positions of taps (taps are special locations in the LFSR that have a connection with the feedback loop);
- Initial state of the LFSR which can be any value except one (all ones for XNOR feedback).

The list of bits position that affects the next state is called the tap sequence.

Table I: Patterns Generated by LFSR

Up counting	Down counting
000	000
001	010
100	110
011	101
101	011
110	100
010	001

The non-tapped bits are shifted from the previous position. The tapped bits are XNORed with the feedback loop before being shifted to the next position. The combination of the taps and their locations can be represented by a polynomial:

Normal LFSR: $g(x) = 1+x^2+x^3$

Inverse LFSR: $g(x) = 1+x+x^3$

The powers of the terms represent the tapped bits, counting from the left. If (and only if) this polynomial is a primitive, then the LFSR is maximal. The LFSR will only be maximal if the number of taps is even. The tap values in a maximal LFSR will be relatively prime. There can be more than one maximal tap sequence for a given LFSR length. By appropriately selecting the tap locations it is always possible to build a maximum-length LFSR of any width with either two or four taps.

B. Comparison with other up/down counters:

The simplest type of synchronous counter is the binary modulo-2^n n bit counter [4]-[5]. For this counter, speed and area are conflicting qualities due to carry propagation. For example, the -bit ripple-carry synchronous counter, one of the simplest counters, has a delay of *O (n)*. Counters with a Manchester carry-chain, carry-look ahead and binary tree carry propagation have delay of *O (log n)* though at the cost of more energy and area. In applications where the count sequence is unimportant [e.g., pointers of circular first-inputs-first-outputs (FIFOs) and frequency dividers], an LFSR counter offers a speed, power, area efficient solution. The delay of an LFSR is nearly independent of its size. Specifically, the LFSR delay consists of a flip-flop delay, an XNOR gate delay, and a feedback loop delay. The feedback loop delay is the propagation delay of the last flip-flop output to the input of the furthest XNOR gate from the last flip-flop. Ignoring secondary effects on the feedback path, the delay of an n-bit maximum length LFSR is *O (1)* and independent of the counter size. These characteristics make LFSRs a suitable counter.

III. DESIGN OF D FLIPFLOP

The most important component of our LFSR Counter Design is D flipflop[4]. The latches and flipflops are the basic building blocks of sequential circuits. In ASIC design environments, latches and flipflops are typically predefined cells specified by the ASIC vendor. The D flipflop is negative edge triggered. The D flipflop combines a pair of D latches (Master and slave). The edge triggered D flipflop has a setup and hold-up time window during which the D inputs must not change. The negative edge triggered D flipflop simply inverts the clock input, so that all the action takes place on falling edge of CLK. By designing D flipflop, power consumption can be compared.

The literature works [6] shows the flipflop design using pass transistors, transmission gates, and NAND gates.

C. Design of D flipflop using NAND gates:

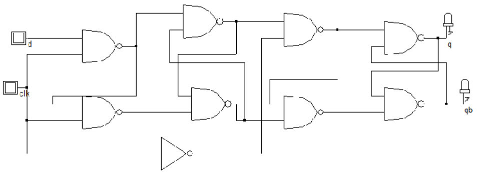

Fig.2. Master Slave D Flip Flop using NAND gate

The basic construction of the Master Slave D Flip Flop is shown in Fig.2. The NAND gate design of D flipflop shows the master and slave section. It has D input and a global clock. The master drives the slave and similarly the slave drives the master.

D. Design of D flipflop using transmission gates:

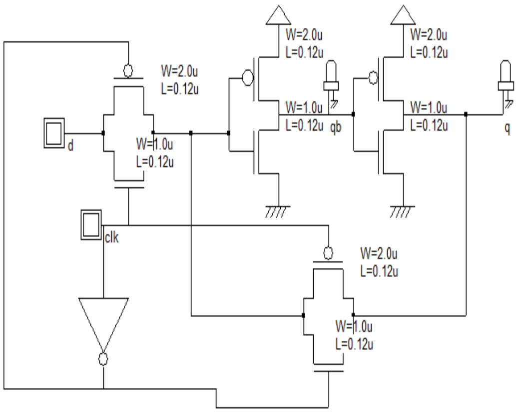

Fig.3. D Flip Flop using transmission gate

At the negative edge of the CLK (clock), transistors T1 and T4 are ON and transistors T2 and T3 are OFF. During this time the slave maintains a loop through two inverters I3, I4 and T4. Thus the previous triggered value from Din is stored in slave.

At the same time master latches next state but as T3 is OFF it is not passed to slave. At the positive clock edge T2 and T3 are turned ON and new latched value passes to slave through the loop of two inverters I1, I2 and T2. When we want to reset the circuit, both the master and slave loops are pulled down to ground.

E. Design of D flipflop using pass transistors:

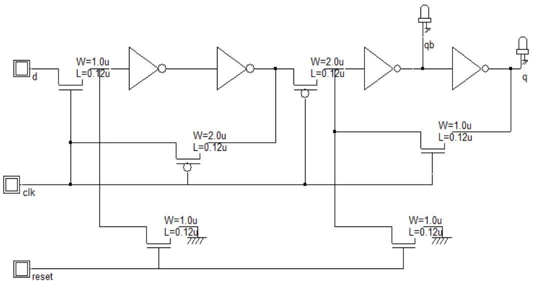

Fig.4. D Flip Flop using pass transistors

The most compact implementation of edge trigger latch is based on inverters and pass transistors [8] as shown in Fig.4. The two chained inverters are in memory state when the PMOS loop transistor is on, that is when CLK=0. Other two chain inverters on the right hand acts in opposite way, and the reset function is obtained by direct ground connection of the master and slave memories, using NMOS devices.

IV. CMOS TOPOLOGIES

The D flipflop is designed using various CMOS topologies such as Classic CMOS, Clocked CMOS, True single phase clocked, Non-precharged true single phase clocked, and 9T flipflop [1]-[3]. The design of each flipflop is shown below. All these designs are drawn using DSCH3, which generates the Verilog code for each schematic. Using the generated Verilog code layout can be drawn for each architecture.

F. Classic CMOS D flipflop:

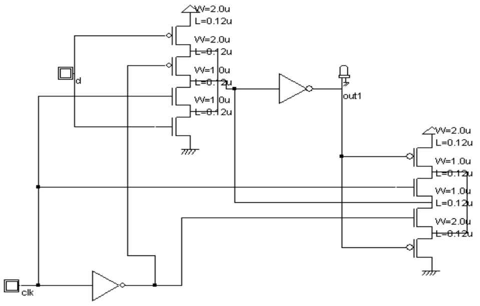

Fig.5.Classic CMOS flipflop

The input stage processes the clock and data signals to ensure correct input signals for the output stage (the single latch on the right). When the clock signal changes from low to high, only one of the output voltages (depending on the data signal) goes low and sets/resets the output latch. If the clock signal continues staying high, the outputs keep their states regardless of the data input and force the output latch to stay in the corresponding state as the input logical zero remains active while the clock is high.

G. Clocked CMOS D Flipflop:

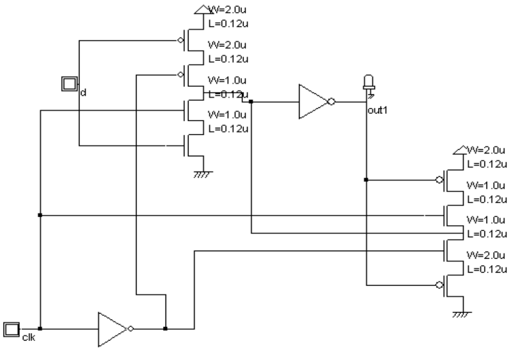

Fig.6. Clocked CMOS flipflop

Clocked CMOS logic has been used for very low power CMOS and/or for minimizing hot electron effect problems in N-FET devices. Clocking transistors allow valid logic output only when CLK is high. Clocking transistors may be at output end of logic trees (maximum performance) or at power supply end of logic trees (maximum protection from hot electrons).

H. True single phase clocked D Flipflop:

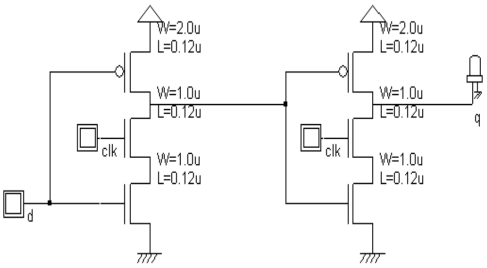

Fig.7.True single phase clocked flipflop

In the true single phase clocking scheme, no clock inversion signal is needed, has a low clock load capacitance, and is glitch free and race free.

I. Non-Precharged True single phase clocked flipflop:

This topology is similar to true single phase clocked logic. But it contains the cascaded stage of it. In this scheme inverting circuitry is additionally added by adding the second stage. At the same time no clock inversion is needed. This reduces floating gate problem in the true single phase clocked topologies.

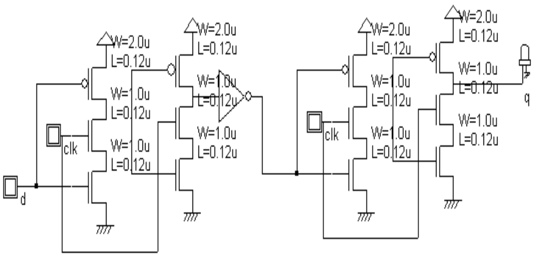

Fig.8. Non- Precharged true single phase clocked flipflop

J. 9T Flipflop:

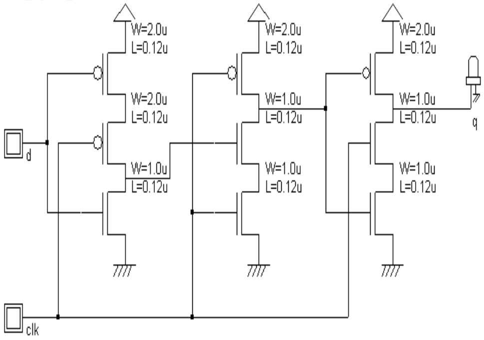

Fig.9. 9T flipflop

Comparing with other logics, this 9T structure reduces the transistor count to a certain extent. This becomes important when the flipflop structure is utilized in large circuitry.

After all the designs are drawn in the schematic, the output dynamic power dissipation for each design is analyzed and a power efficient one is chosen. The clocked CMOS [6] has the least power dissipation of all. But at the same time, it suffers from high delay. When compared on area basis TSPC has least transistor count. But it has floating gate problem and hence could not be considered for the design of LFSR counter. After the D flipflop is designed, the best chosen topology is used to design the LFSR counter.

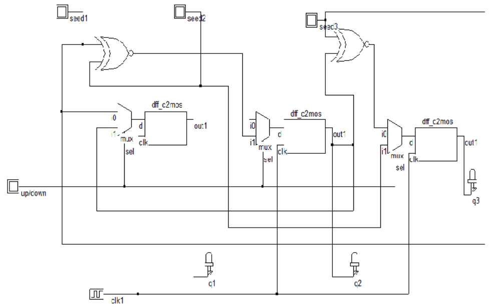

Fig.10.LFSR designed using clocked CMOS logic

V. LAYOUT GENERATION

Before implementing the whole circuit, a gate-level schematic in DSCH3 [2] is generated. DSCH3 program is a logic editor and simulator used to validate the architecture of logical circuit, before microelectronics started. It provides user friendly environment for hierarchical logic design and fast simulation with delay analysis, which allows design and validation of complex logic structures. After successful simulation the above designs of D Flip Flop with different components is implemented using Microwind 3.1 CMOS layout tool for its ease of use and availability.

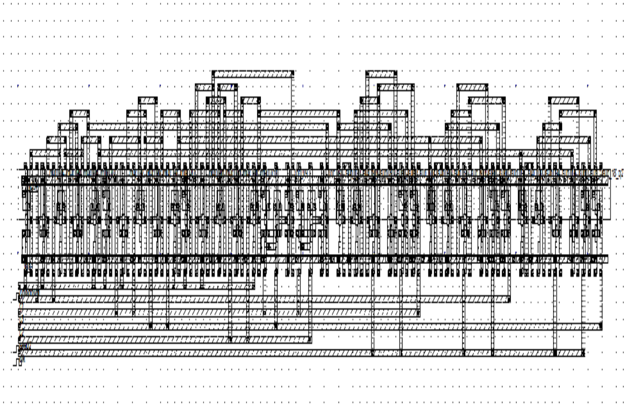

Fig.11. Layout of LFSR designed using clocked CMOS D flipflop

VI. SIMULATION RESULTS

The schematic is drawn using the DSCH3 [10] and the output for the corresponding schematic is viewed in the timing diagram. For the power calculation, the schematic is converted to a Verilog code which can be generated using DSCH3 itself. The Verilog code is then simulated using Microwind for layout generation. Using the layout window, power, area and delay can be found out. The following table gives the comparison of all the parameters when the LFSR is designed using various topologies.

Table III: Comparison of LFSR designed using various CMOS topologies

Logic	Power (µW)	Delay (ps)	Transistor Count
Classic	107	96	54
C^2MOS	102	220	54
TSPC	105	120	45
NPTSPC	123.5	128	48
9T	231	142	63

Microwind EDA tool was used for the layout and simulation of the counter using BSIM4 MOSFET model in 120 nm technology. Performance characteristics such as static power dissipation, dynamic power dissipation, propagation delay and power delay products in static and dynamic conditions were observed. The power results are compared to obtain a power efficient structure.

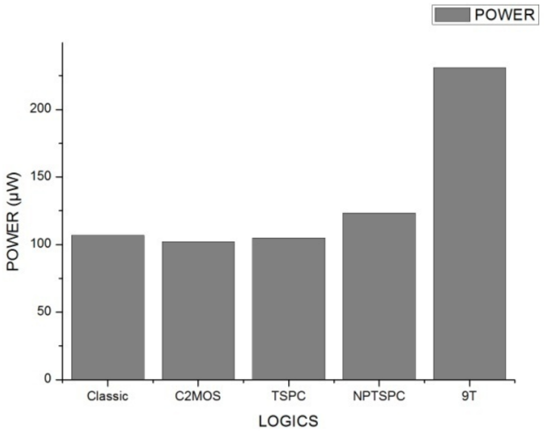

Fig.12. Graph showing the comparison of power dissipation for the LFSR designed using various CMOS logics

Table III: physical aspects of MOS transistors for CMOS technique

Physical Aspect	NMOS Transistor	PMOS Transistor
Channel width(µm)	0.240	0.720
Channel length(µm)	0.120	0.120
Aspect ratio	2	6

VII. CONCLUSION

This paper concludes that LFSR counter is best implemented using the clocked CMOS logic. In this method, the number of transistors required is minimum i.e. 54, power consumption is 102(µW).Thus it is preferable over other logics in maintaining the logic density in power optimization, reducing the propagation delay & glitches.

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ACKNOWLEDGMENT

The authors acknowledge the contributions of the students, faculty of Velalar College of Engineering and Technology for helping in the design of test circuitry, and for tool support. The authors also thank the anonymous reviewers for their thoughtful comments that helped to improve this paper. The authors would like to thank the anonymous reviewers for their constructive critique from which this paper greatly benefited.

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